AMENDMENTS TO THE SPECIFICATION

Please replace the present title with the following amended title:

~~LEVEL CONVERSION CIRCUIT~~LEVEL CONVERSION CIRCUIT WITH IMPROVED MARGIN OF LEVEL SHIFT OPERATION AND LEVEL SHIFTING DELAYS

Please replace the paragraph no. 76 with the following amended paragraph:

FIG. 7 is a diagram showing a level shift circuit 6 according to an embodiment of the present invention. The level shift circuit 6 of the present invention changes the signal level in a first logic circuit 4 fed from a first power supply (VDDL) to the signal level in a second logic circuit 5 fed from a second power supply (VDDH), and is provided with a level shift core circuit 1. The first logic circuit 4 supplies the level shift core circuit 1 with signals INL and INLB at the first power supply level, and thereby conversion from first to second power supply level takes place.

Please replace the paragraph no. 77 with the following amended paragraph:

The level shift circuit 6 of the present invention is further provided with, in addition to the level shift core circuit 1, a control circuit 2 fed from the second power supply and a pull-up and/or pull-down circuit 3 also fed from the second power supply.

Please replace the paragraph no. 102 with the following amended paragraph:

A description will be given of a level shift circuit 6 according to the second embodiment of the present invention. According to this embodiment, the pull-down function of the pull-up and/or pull-down circuit 3 in the first embodiment can be omitted as shown in FIG. 18. In the circuitry exemplified in FIG. 18, a pull-up circuit of FIG. 20 may be used in combination with the control circuit 2 shown in FIG. 6 or 19, or a pull-up circuit 3-1 of FIG. 22 may be used in combination with a control circuit shown in FIG. 21. The control circuit shown in FIG. 21 may be substituted with another control circuit that outputs the control signals C0 and C1, as, for example, the one shown in FIG. 6 or 19. However, when such a substitute has been provided, the pull-up circuit 3-1 shown in FIG. 22 is replaced with the pull-up circuit 3-1 shown in FIG. 20 with a polarity opposite to that of the circuit 3-1 of FIG. 22.

Please replace the paragraph no. 106 with the following amended paragraph:

The pull-down circuit 3-2 of FIG. 27 having an NMOS (transistor) construction may be substituted with the pull-down circuit 3-2 of FIG. 28 having a PMOS (transistor) construction. In other words, when the level shift core circuit 1 of FIG. 8 and the control circuit 2 of FIG. 5, instead of the circuit 2 of FIG. 4 or 26, are employed, a level shift circuit 6 can be constructed by replacing the pull-down circuit 3-2 shown in FIG. 27 with that shown in FIG. 28. However, the combination of these circuits has to be determined according to their polarity.

Please replace the paragraph no. 112 with the following amended paragraph:

As can be seen in FIG. 29, a level shift circuit 6 according to the third embodiment of the present invention comprises a pull-up circuit 3-1 for performing pull-up operation based on signals INL or INLB output from the first logic circuit 4 fed from the first power supply VDDL, and a level shift core circuit fed from the second power supply VDDH which receives the signal(s) INL and/or INLB as well as outputting (a) signal(s) OUTH and/or OUTHB. The signal(s) OUTH and/or OUTHB are/is output to the second logic circuit fed from the external second power supply.

Please replace the paragraph no. 114 with the following amended paragraph:

In the following, a description will be given of the operation of the level shift circuit 6 according to the third embodiment of the present invention. It is assumed that, as shown in the timing chart of FIG. 13, INL is low, INLB is high, OUTH is low, and OUTHB is high in the initial state. When INL (an input signal to the pull-up circuit, and referred to as C0) output from the first logic circuit 4 has changed to high, the NMOS connected to OUTH turns on in the pull-up circuit 3-1 and pulls up OUTH. At this time, since INLB (an input signal to the pull-up circuit, and referred to as C1) is low, the other NMOS connected to OUTHB is off. Subsequently, when OUTHB has been pulled down to low due to the operation of the level shift core circuit 1, high CO is output. Accordingly, the NMOS of the pull-up circuit 3-1 turns off, thereby terminating the pull-up operation. As a result, INL becomes high, INLB becomes low, OUTH becomes high, and OUTHB becomes low.

Please replace the paragraph no. 117 with the following amended paragraph:

In FIG. 32, the level shift circuit 6 has an additional function to generate control signals for the PMOS switches of the level shift core circuit shown in FIG. 16.

Please replace the paragraph no. 128 with the following amended paragraph:

In this embodiment, the level shift core circuit 1 of FIG. 33 used in the fourth embodiment is employed, and both the pull-up and pull-down circuits are omitted as shown in FIG. 38. In the fifth embodiment, the same level shift core circuit 1 and control circuit 2 as described previously in the fourth embodiment can be utilized. Concretely, the level shift core circuit 1 shown in FIG. 33 and the control circuit 2 shown in FIG. 34 or 36 are adopted. That is, the level shift circuit 6 of the fifth embodiment comprises the level shift core circuit 1 and the control circuit 2. The control circuit 2 is fed from the second power supply VDDH and receives the signals INL and INLB output from the first logic circuit as well as outputting control signals (C4, C5, etc.) for controlling the level shift core circuit 1. The level shift core circuit 1, fed from the second power supply VDDH, receives the signals output from the control circuit and the signals INL and INLB from the first logic circuit as well as outputting the signals OUTH and OUTHB for controlling the second logic circuit. The signals OUTH and OUTHB output from level shift core circuit are supplied to the control circuit. As just described, such control circuit as needs no inverter circuit to output the control signals C4 and C5 may be employed.

Please replace the paragraph no. 129 with the following amended paragraph:

The level shift circuit 6 of the fifth embodiment operates as shown in the timing chart of FIG. 37.